

Answer only four of the following problems:

Problem 1:

Compute the end-to-end delay for virtual circuit packet switching and datagram packet switching. Assume there are no acknowledgments. Ignore processing delay at the nodes. There are four hops, a 0.001 propagation delay per hop in seconds, a 3200 bit message, a 9600 bps data rate and a packet size of 1024-bits including 16-bit header. The call setup time is 0.2 seconds.

Problem 2:

Regarding protocol data unit (PDU) in the TCP/IP architecture, exactly one PDU in layer N is encapsulated in a PDU at layer (N-1). It is also possible to break one N-level PDU into multiple (N-1)-level PDUs (segmentation) or to group multiple N-level PDUs into one (N-1)-level PDU (blocking).

- 2.1 In the case of segmentation, is it necessary that each (N-1)-level segment contain a copy of the N-level header?
- 2.2 In the case of blocking, is it necessary that each N-level PDU retain its own header, or can the data be consolidated into a single N-level PDU with a single N-level header?

Problem 3:

- 3.1 Using a schematic, describe CSMA in its three cases: non-persistent, 1-persistent, and p-persistent.
- 3.2 Using a schematic, describe the CSMA/CD operation for four stations A, B, C, and D showing at least one collision.

Problems 4:

For 1-persistent CSMA the relation between S and G is given by:

$$S = [G (1 + G) e^{-G}] / (G + e^{-G})$$

Plot this relation for $0.01 \leq G \leq 1.0$, and find the channel capacity.

Problem 5:

Complete the following time sequence diagram

