COLLEGE OF ENGINEERING & TECHNOLOGY

Department: Computer Engineering

Lecturers: Prof. Dr. Magdy Saeb

Course: Final Exam. (Computing Systems)

Course No. CC513

Date: June 2007 **Time:** 120 minutes **Grade:** 40 marks

Answer only four of the following problems:

Problem 1: ***25 points***

1.1 Compare VLIW architectures with superscalar architectures.
a) Show the similarities and differences
b) Show the advantages and disadvantages of the two approaches.

1.2 Consider a sequence of ten instructions and show how it passes through a four and six-stage pipeline respectively. Draw a figure for each of the two cases.
How many clock cycles are needed in each case?
Assuming that the second machine cycle time is 0.9 times the cycle time of the first machine.
Which is the shorter execution time of the sequence?
Can we conclude that increasing number of stages always provides improved performance? Bring arguments. (Consider that no hazards occur).

Problem 2: ***25 points***

Consider a machine based on a RISC instruction set, the timings for each micro-operation are given in the following table.

Micro-operation	Time in nano seconds (nsec)
Read from Instruction Cache	10
Increment Program Count	4
Decode	7
Floating-Point Operation	60
Integer/Logic Operation	20
Control Flow Operation	10
Writing in Register File	6
Accessing Data Cache	10

You are asked to design a pipeline for such a machine. For simplicity, we assume that any micro-operation can be divided into any number of stages, given that any division adds a 2nsec overhead on every new stage. Also, it is required that the latency in your designed pipelined would not be more than 1.25 the latency in a non-pipelined machine.

(a) Some of these micro-operations can be performed in parallel, state those ones that can be performed in parallel.
(b) Calculate the number of stages and the maximum throughput.

Note: In RISC machines only the load/store instructions access the data cache and only the Floating-Point and Integer /Logic Operations require a register file access at write back.

Problem 3: ***25 points***

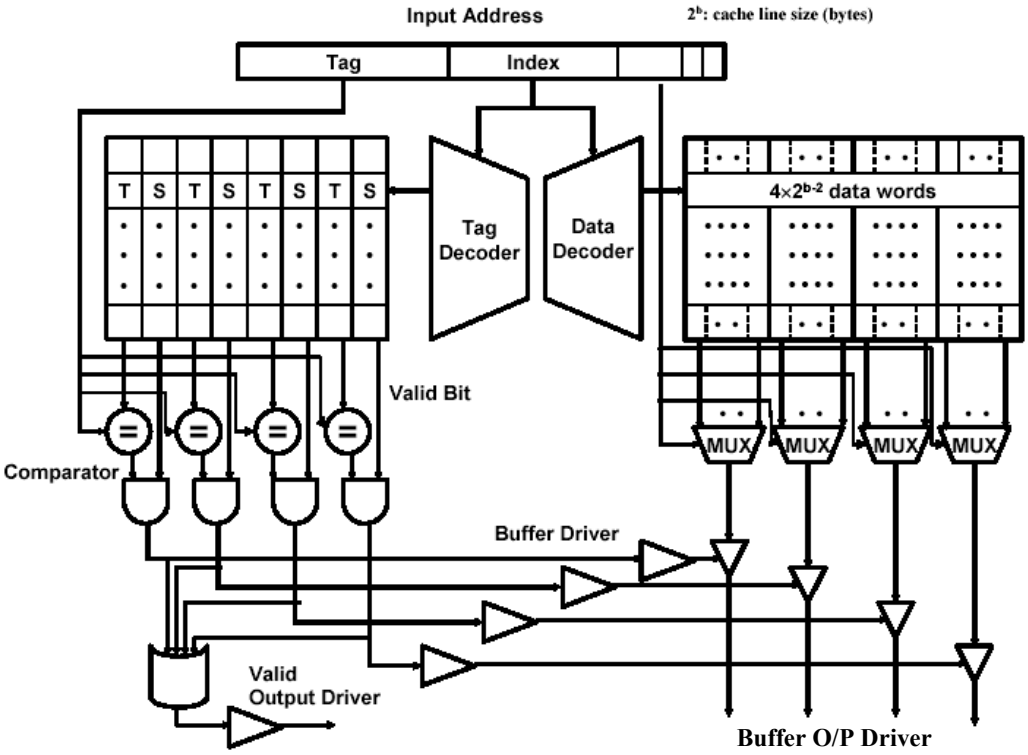
Consider a 256-KB cache with 8-word cache lines. The address is 32 bits, and the cache access is word-aligned. The MUX selects one word out of the 8-words in a cache line.

a. Fill in the table for the four-way set-associative (SA) cache shown in figure, using the delay equations given in the table below. Assume that two bits are reserved for the "Status" field

and that the delay for the two-input AND gate is 500 psec and for the 4-input gate, a delay of 1000 ps.

b. Show the critical path in the following hardware and compute the memory access time in pico seconds.

c. If the processor to which this cache memory will be coupled works at 150MHz, how many cycles would one memory access require?



Component	Delay equation (ps)		SA (ps)
Decoder	200×(# of index bits) + 1000	Tag	
		Data	
Memory array	200×$\log_2$ (# of rows) + 200×$\log_2$ (# of bits in a row) + 1000	Tag	
		Data	
Comparator	200×(# of tag bits) + 1000		
N-to-1 MUX	500×$\log_2$ N + 1000		
Buffer driver	2000		
Data output driver	500×(associativity) + 1000		
Valid output driver	1000		

Problem 4: ***25 points***

Consider a two-level memory hierarchy, M1 and M2. Denote the hit ratio of M1 as h. Let t1 and t2 be the access time in cycles for M1 and M2, respectively. You are asked to choose between direct mapping implementation and 4-way set-associative implementation for M1. The direct mapping 256 Kbyte-memory takes 13300 psec for maximum combinational delay. The 4-way set associative takes three processor-cycles to access one word. The second level, M2, is a main memory with a 4Mbyte capacity and require 12 processor-cycles for one access.

(a) If hit ratio for the direct mapping implementation is given by 0.8, what is the lower bound for the hit ratio (h) that would make the choice of the 4-way set associative implementation interesting?
(b) What is the effective memory-access time ta of this hierarchy?
(c) Let r = t2/t1 be the speed ratio of the two memories. Let E = t1/ta be the access efficienct of the memory system. Express E in terms of r and h.
(d) Plot E against h for the 4-way set-associative implementation choice.
(e) What is the required hit ratio h to achieve an access efficiency of more than 95%?

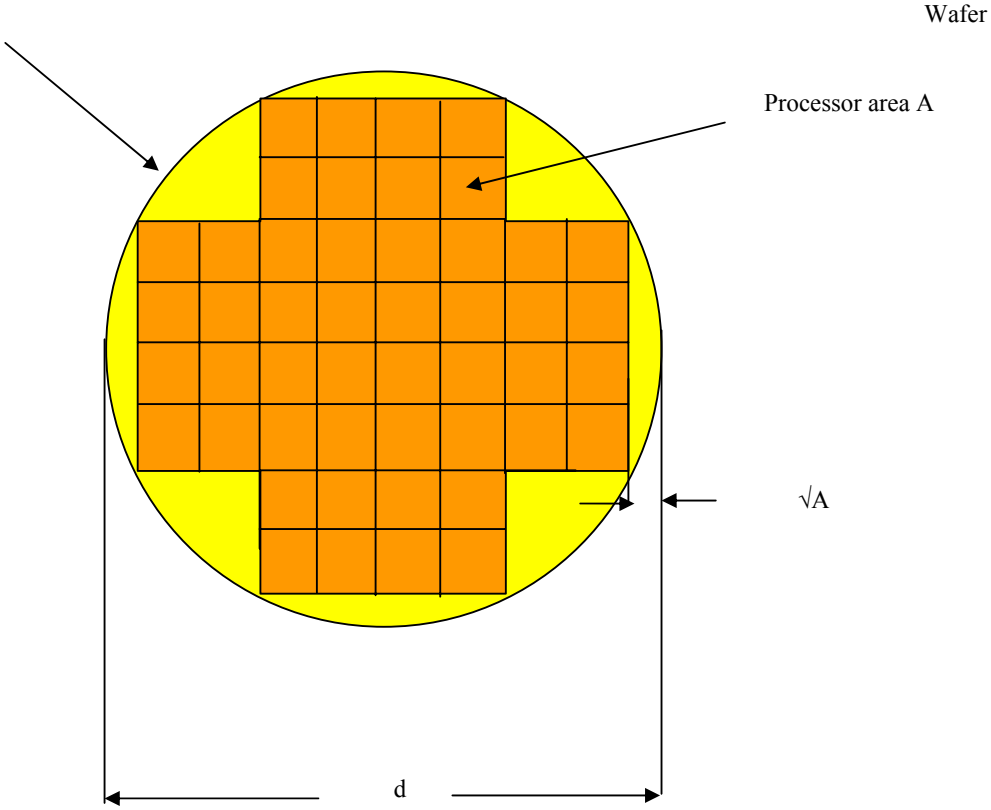
Problem 5: ***25 points***

(a) Construct a 16-input Omega network using 2x2 switch modules in multiple stages. How many stages are there ? Hint: The number of statges as equal to $\log_2$(number of inputs)
(b) How many switches are there in this network?
(c) What is the main problem of the omega network? How can you rectify this problem?
(d) In which of the Flynn's classified architectures are these multistage networks used?
(e) What is the advantage of such an interconnection compared to the fully connected network?

Problem 6: ***25 points***

A wafer diameter (d) is 21cm; its cost is $5000, and its defect density ($\rho_{D)}$ is 1defect/cm^2.
Assuming that the area consumed by one instruction is a_i and it is approximately equal to 0.01cm2.
Find the maximum number of instructions that can be fitted on the processor area (A), such that its cost does not exceed $50.

Hint: The yield (Y) is given by $Y = e^{(-\rho_D A)}$ *, where* ρ_D *is the defect density.*
The yield is the ratio of the good dies (N_G) *to the total number of dies (N).*



Good Luck, …we all need some! ☺